Dual N-Channel 20V(D-S) Enhancement Mode Mosfet

GENERAL DESCRIPTION

The 8810 Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 20m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 21m\Omega @ V_{GS}=4.0V$
- $R_{DS(ON)} \leqq 22m\Omega @ V_{GS}=3.1V$
- $R_{DS(ON)} \leqq 24m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

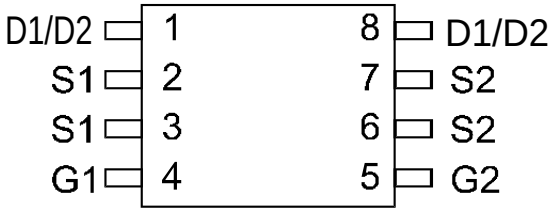
APPLICATIONS

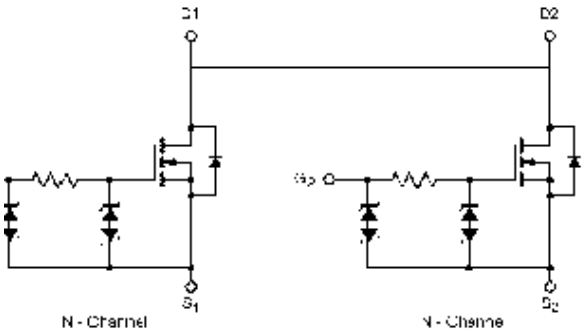
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

(TSSOP-8)

Top View





The **Ordering Information**: 8810 (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	10 secs	Maximum	Unit
Drain-Source Voltage		V_{DSS}	20		V
Gate-Source Voltage		V_{GSS}	±12		V
Continuous Drain Current(tJ=150℃)	T_A=25℃	I_D	6.5	5.2	A
	T_A=70℃		5.5	3.5	
Pulsed Drain Current		I_{DM}	30		A
Continuous Source Current (Diode Conduction)		I_S	1.5	1.0	A
Maximum Power Dissipation	T_A=25℃	P_D	1.5	1.0	W
	T_A=70℃		0.96	0.64	
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	70	100	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.6	0.8	1.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±10	uA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	μA
		V_{DS}=20V, V_{GS}=0V T_J=70℃			25	
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=4.5V, I_D=7.0A		16.5	20	mΩ
		V_{GS}=4V, I_D= 7.0A		17	21	
		V_{GS}=3V, I_D= 6.0A		18	22	
		V_{GS}=2.5V, I_D= 5.5A		20	24	
V_{SD}	Diode Forward Voltage	I_S=1.5A, V_{GS}=0V		0.73	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=10V, I_D=6.5A		18	22	nC
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=6.5A		10	12	
Qgs	Gate-Source Charge			2.2		
Qgd	Gate-Drain Charge			3.6		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V,f=1MHz		245	300	pF
Coss	Output Capacitance			90		
Crss	Reverse Transfer Capacitance			26		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=10V, R_L =10Ω I_D=1A, V_{GEN}=4.5V R_G=6Ω		140	200	ns
t_r	Turn-On Rise Time			210	250	
$t_{d(off)}$	Turn-Off Delay Time			390	450	
t_f	Turn-Off Fall Time			220	260	

Notes:Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

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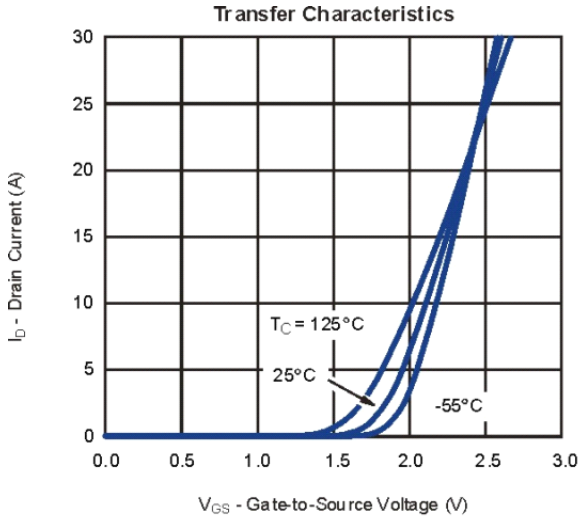

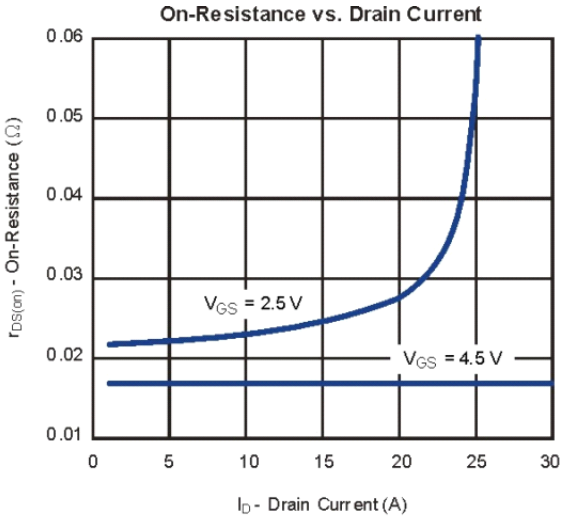

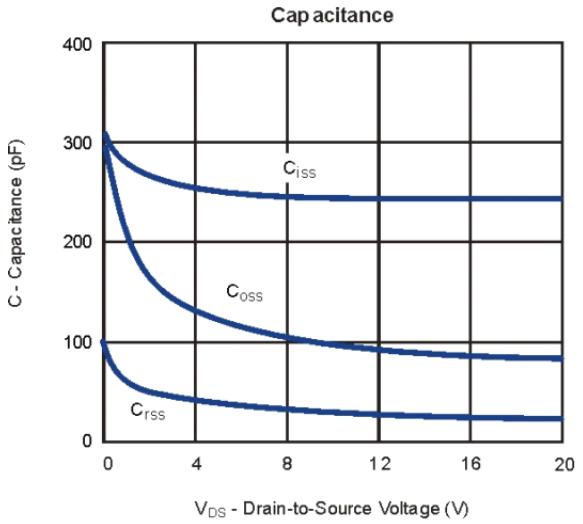

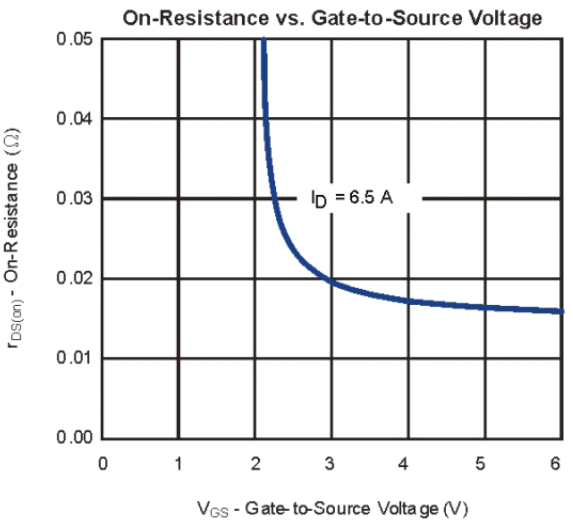

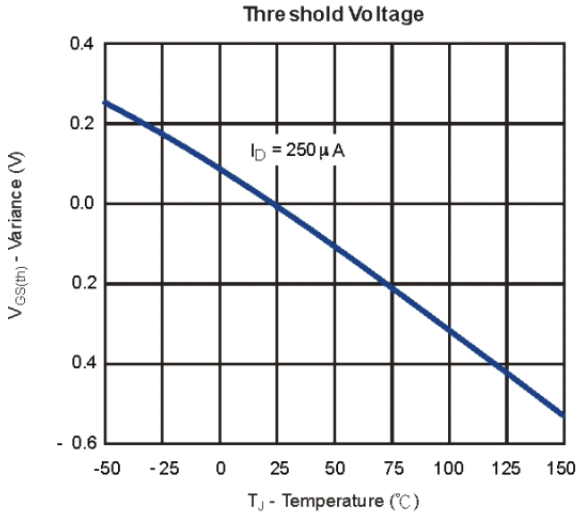

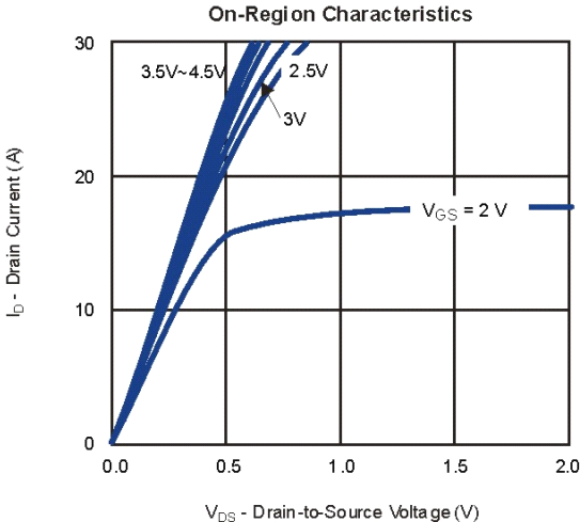

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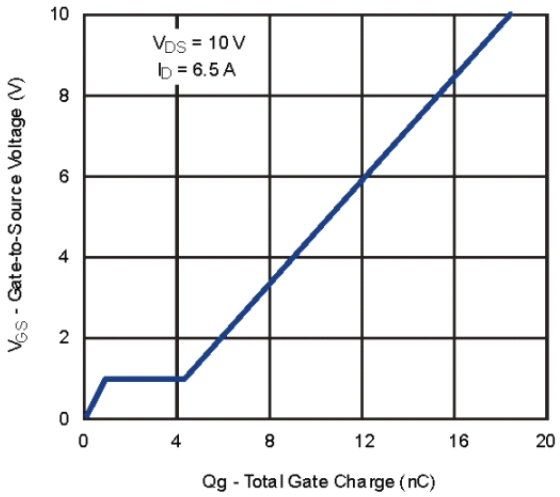
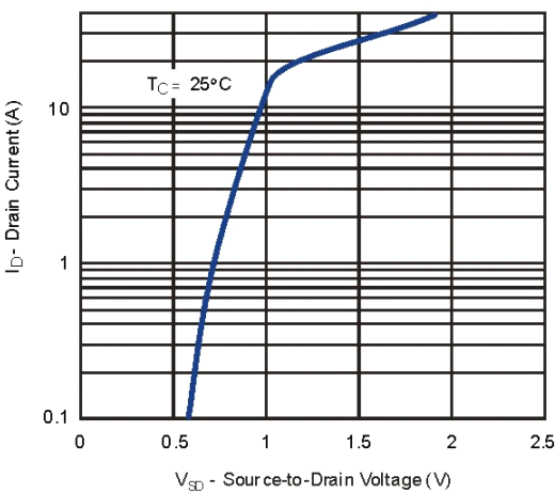
Typical Characteristics (T_J =25℃ Noted)

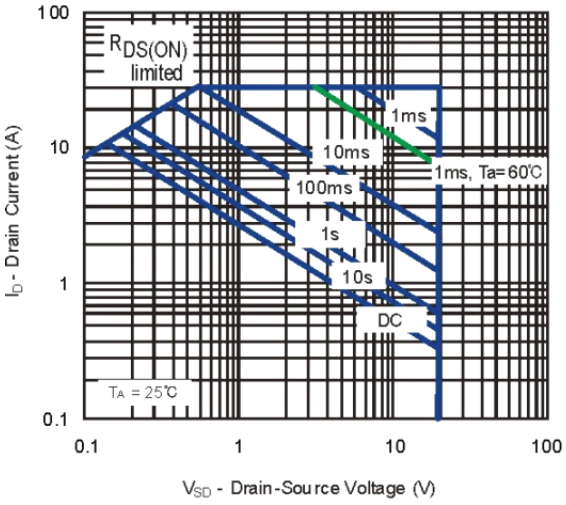
Gate Charge



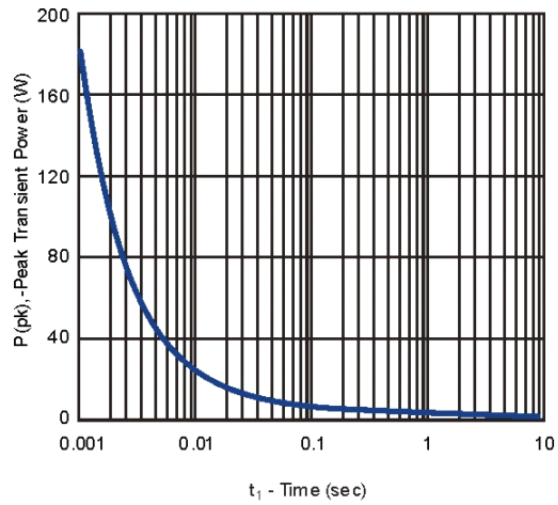
On-Resistance vs. Drain Current



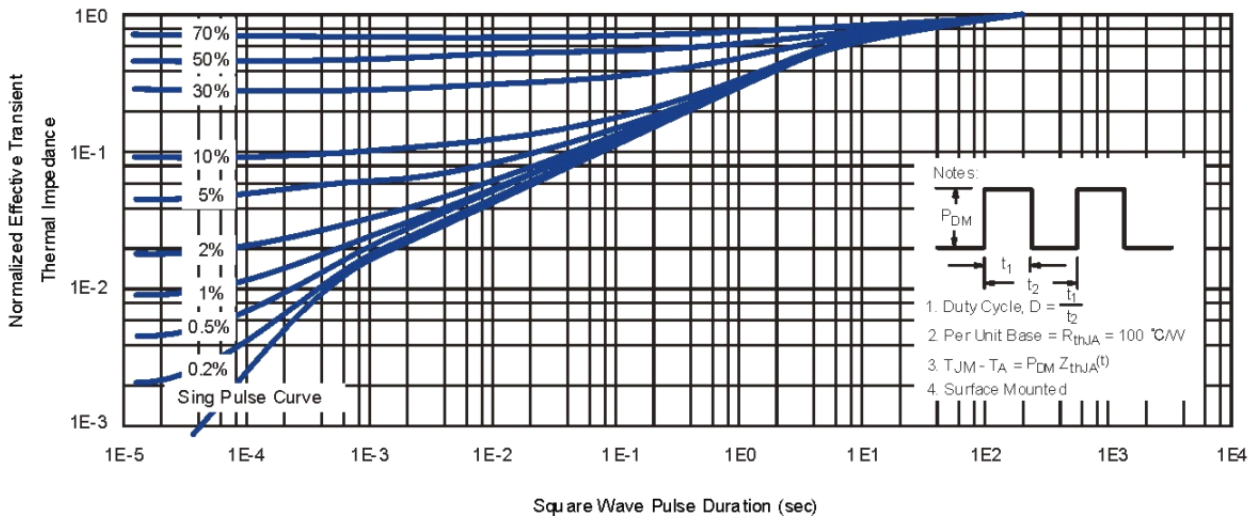
Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



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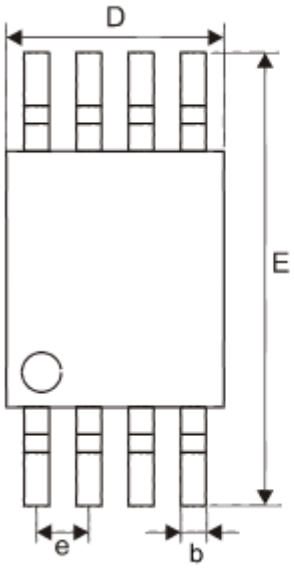
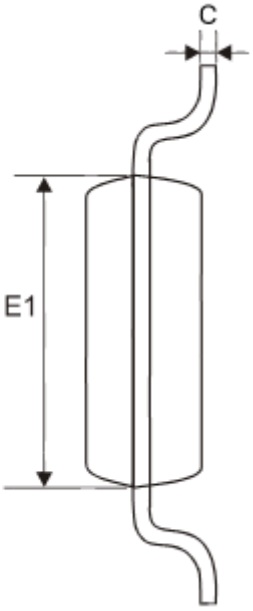
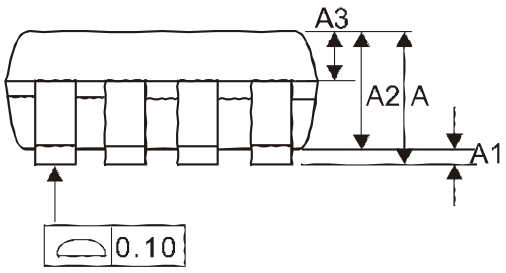
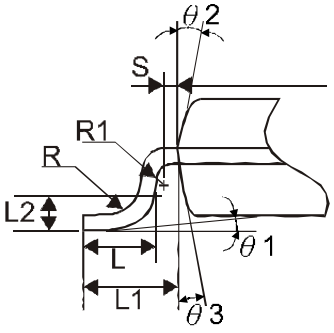
TSSOP-8 Package









SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	-	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.34	0.54
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L1	1.00REF	
L2	0.25BSC	
R	0.09	-

NNote: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.